

## Libraries

Name	Process	Form Factor
RGO_GF40_25V33_LP_20C_FT	LP	Staggered CUP
RGO_GF40_25V33_LP_40C_FT	LP	Inline CUP

## Summary

The 3.3V GPIO FT library provides general purpose bidirectional I/O cells that are fault tolerant. These programmable, multi-voltage I/O's give the system designer the flexibility to design to a wide range of performance targets.

This 40nm library is available in both staggered CUP and inline CUP wire bond implementations with a staggered flip chip option.

To design an operational I/O power domain with these cells, an additional library is required – 3.3V Wide Range GPIO. That library contains a full complement of cells to support the assembly of a functional pad ring by abutment. That set includes an input-only buffer, isolated analog I/O, and power / ground cells along with corner and spacer cells. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

### ESD Protection:

- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

### Machine Model ESD Protection:

Machine Model (MM) is not required for ESD qualification of IC's per JESD47. For customers that still request it, Aragio provides the SCR variant of the 5VT GPIO that passes the 200V qualification test as defined in JESD22-A115C. The non-SCR variant passes 100V.

### Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of  $\pm 100\text{mA}$  @  $125^\circ\text{C}$

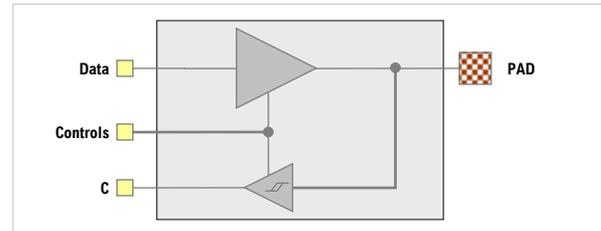
## Cell Size & Form Factor

- Staggered (pad-limited) –  $28\mu\text{m} \times 200\mu\text{m}$
- Inline (core-limited) –  $58\mu\text{m} \times 100\mu\text{m}$

## Recommended operating conditions

Description	Min	Nom	Max	Units
$V_{\text{VDD}}$ Core supply voltage	0.90	1.0	1.10	V
	0.99	1.1	1.21	V
	1.08	1.2	1.26	V
$V_{\text{DVDD}}$ I/O supply voltage	2.97	3.3	3.63	V
	2.70	3.0	3.30	V
	2.52	2.8	3.08	V
$T_{\text{J}}$ Junction temperature	-40	25	175	$^\circ\text{C}$
	2.25	2.5	2.75	V
	1.62	1.8	1.98	V
$V_{\text{PAD}}$ Voltage at PAD	$V_{\text{DVSS}} - 0.3$	-	$V_{\text{DVDD}} + 0.3$	V

## FRx\_BI\_SDS\_33V\_STB & FRx\_BI\_SDS\_33V\_STB\_SCR



## Bidirectional GPIO Driver Features

- Fault tolerant - no current flow when  $DVDD = 0\text{V}$  at  $V_{\text{PAD}} \leq 3.63\text{V}$
- Multi-Voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V)
- LVCMOS / LVTTTL input with selectable hysteresis
- Programmable drive strength (rated 2mA to 12mA)
- Selectable output slew rate
- Optimized for EMC with SSO factor of 8
- Open-drain output mode
- Programmable input options (hi-Z/pull-up/pull-down/repeater)
- Power-On Start (POS) capable
- Power sequencing independent design with Power-On Control

In full-drive mode, this driver can operate to frequencies in excess of 100MHz with 15pF external load and 125 MHz with 10pF load. Actual frequency limits are load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

## Characterization Corners

Nominal VDD	Model	VDD	DVDD <sup>[1]</sup>	Temperature
1.2	FF	+5%	+10%	-40 $^\circ\text{C}$
	FFF	+5%	+10%	125 $^\circ\text{C}$
	FFF	+5%	+10%	150 $^\circ\text{C}$
	FFF	+5%	+10%	175 $^\circ\text{C}$
	TT	nominal	nominal	25 $^\circ\text{C}$
	SS	-10%	-10%	-40 $^\circ\text{C}$
	SS	-10%	-10%	125 $^\circ\text{C}$
	SS	-10%	-10%	150 $^\circ\text{C}$
	SS	-10%	-10%	175 $^\circ\text{C}$
	1.1 / 1.0	FF	+10%	+10%
FFF		+10%	+10%	125 $^\circ\text{C}$
FFF		+10%	+10%	150 $^\circ\text{C}$
FFF		+10%	+10%	175 $^\circ\text{C}$
TT		nominal	nominal	25 $^\circ\text{C}$
SS		-10%	-10%	-40 $^\circ\text{C}$
SS		-10%	-10%	125 $^\circ\text{C}$
SS		-10%	-10%	150 $^\circ\text{C}$
SS	-10%	-10%	175 $^\circ\text{C}$	

<sup>[1]</sup> DVDD = 1.8, 2.5, 2.8, 3.0 and 3.3V

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